

MS-7676 Ver: 3.0 m-ATX : 245 X 245mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(Z68)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI *1

TPM Header *1(debug only)

on BOARD BUZZER

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BOM:

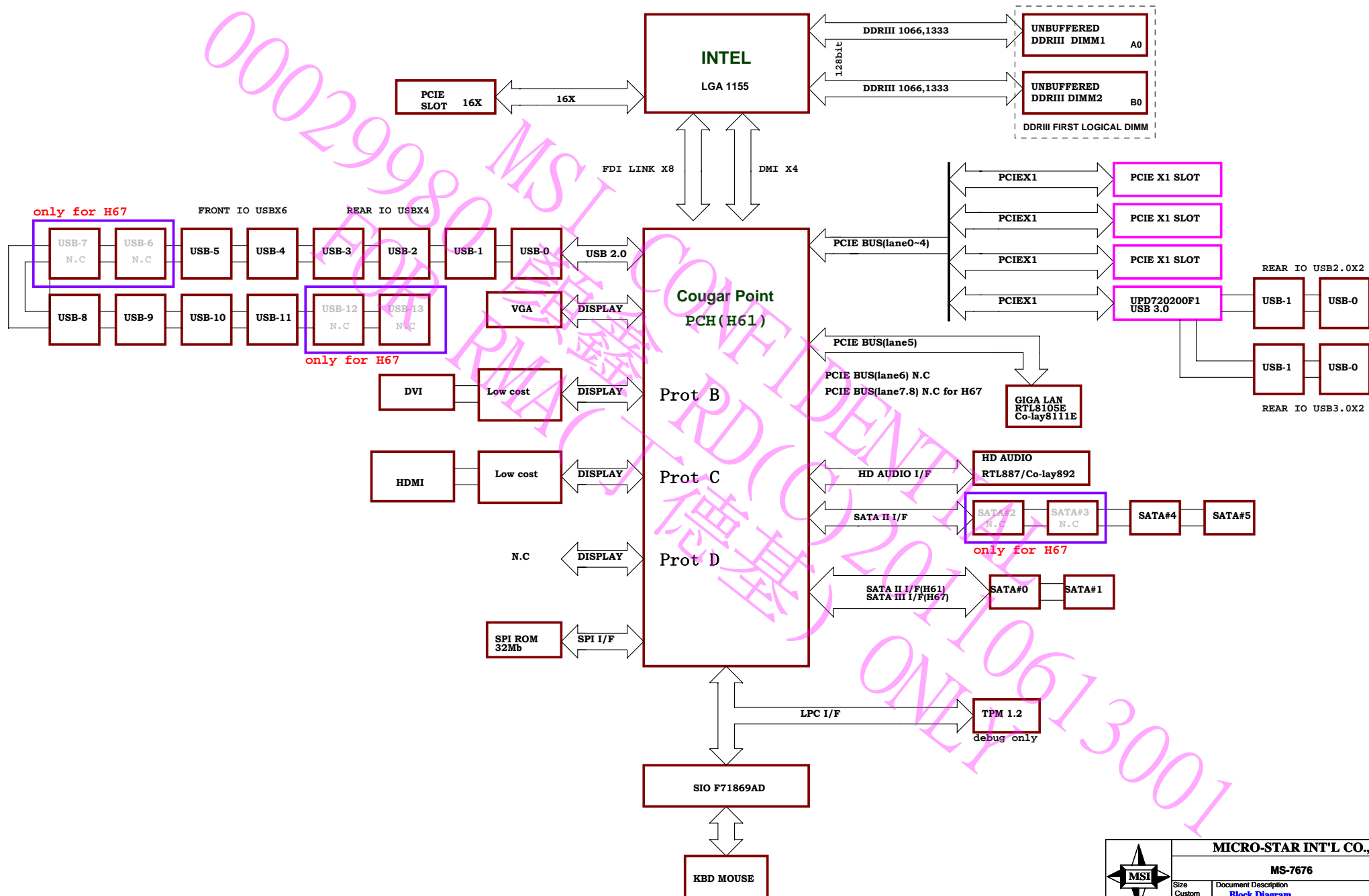
- 1.H67 Full Spec(mil)
- 2.H61 Full Spec(mil)
- 3.H61 common Spec(mil)

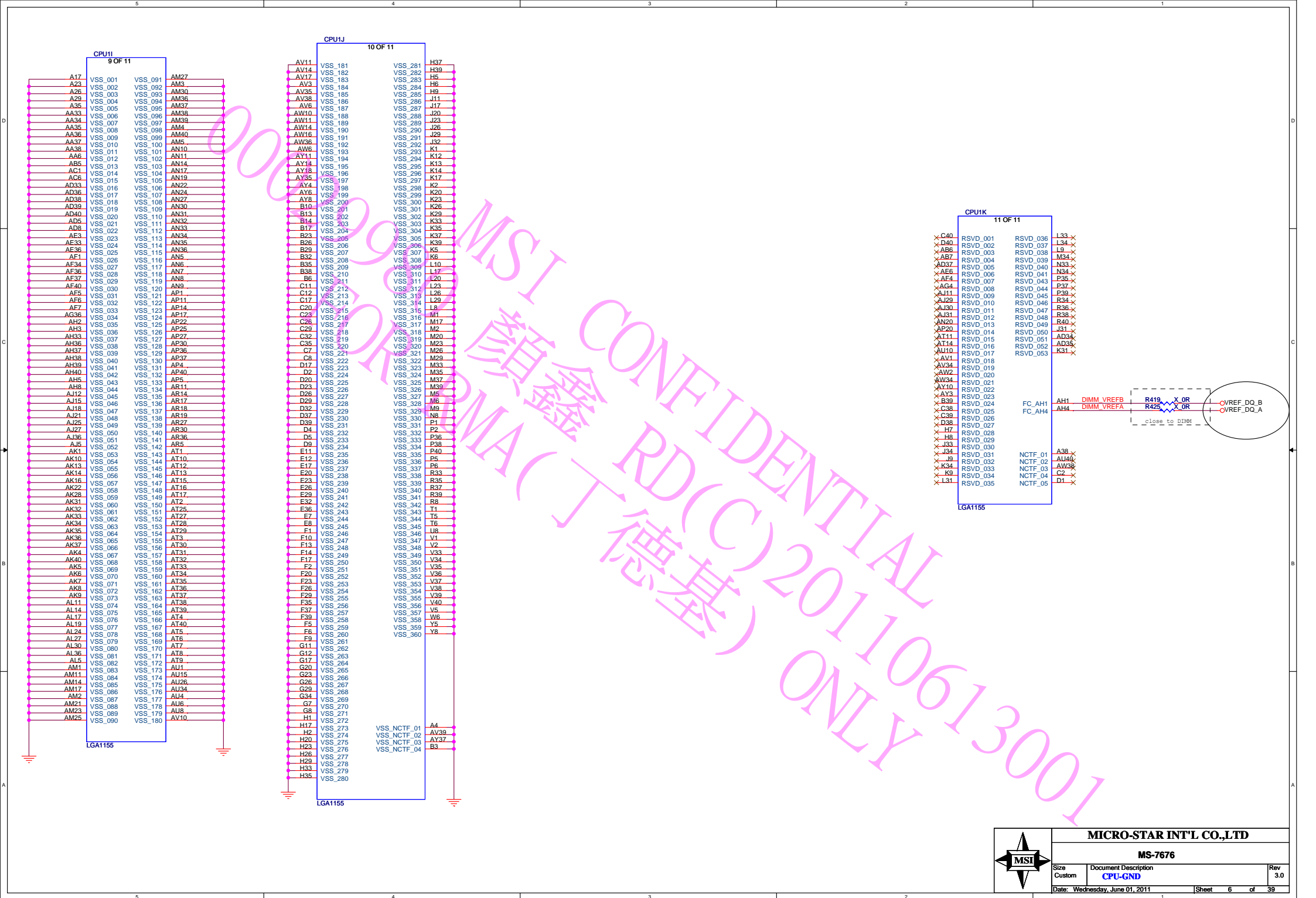


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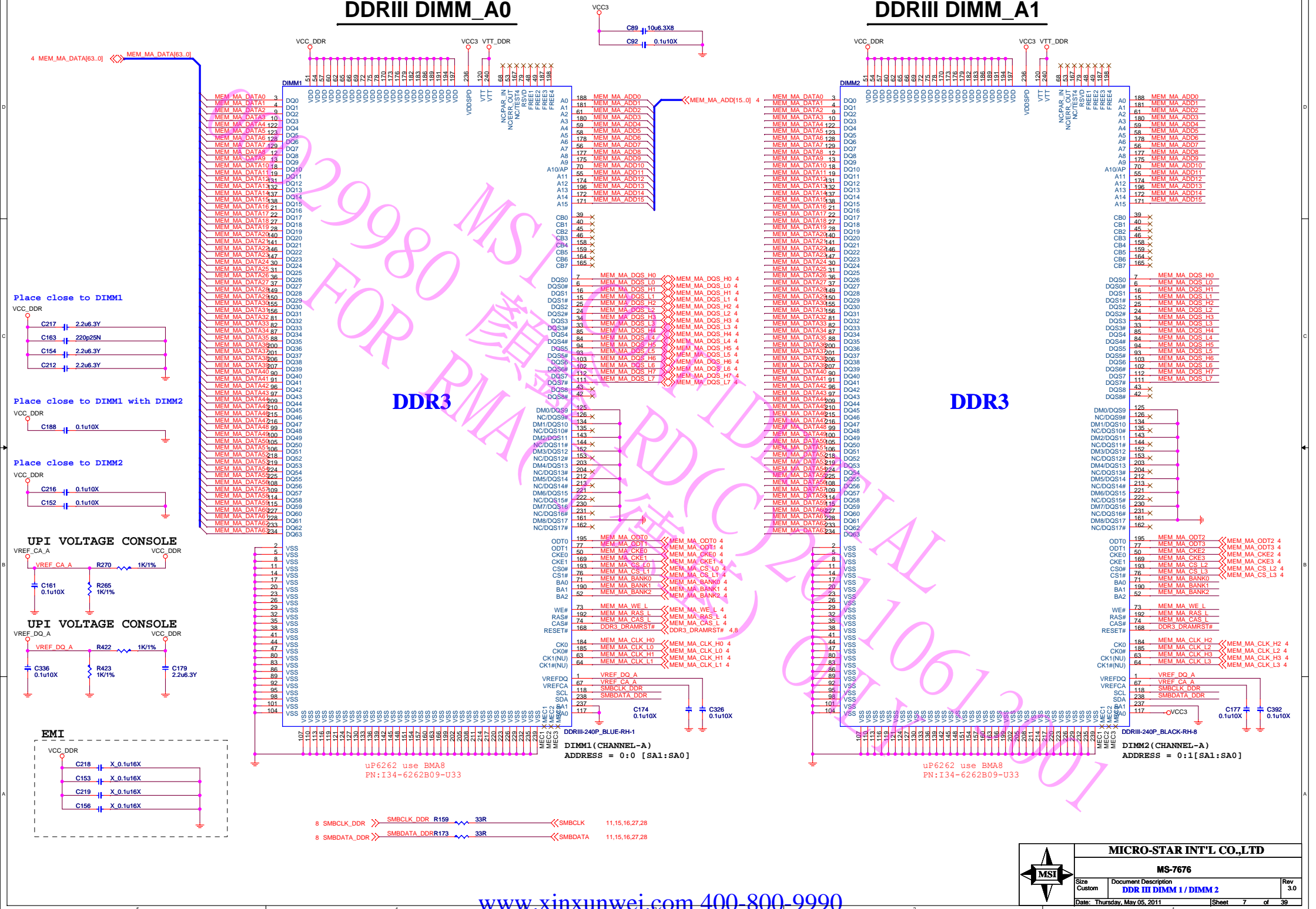
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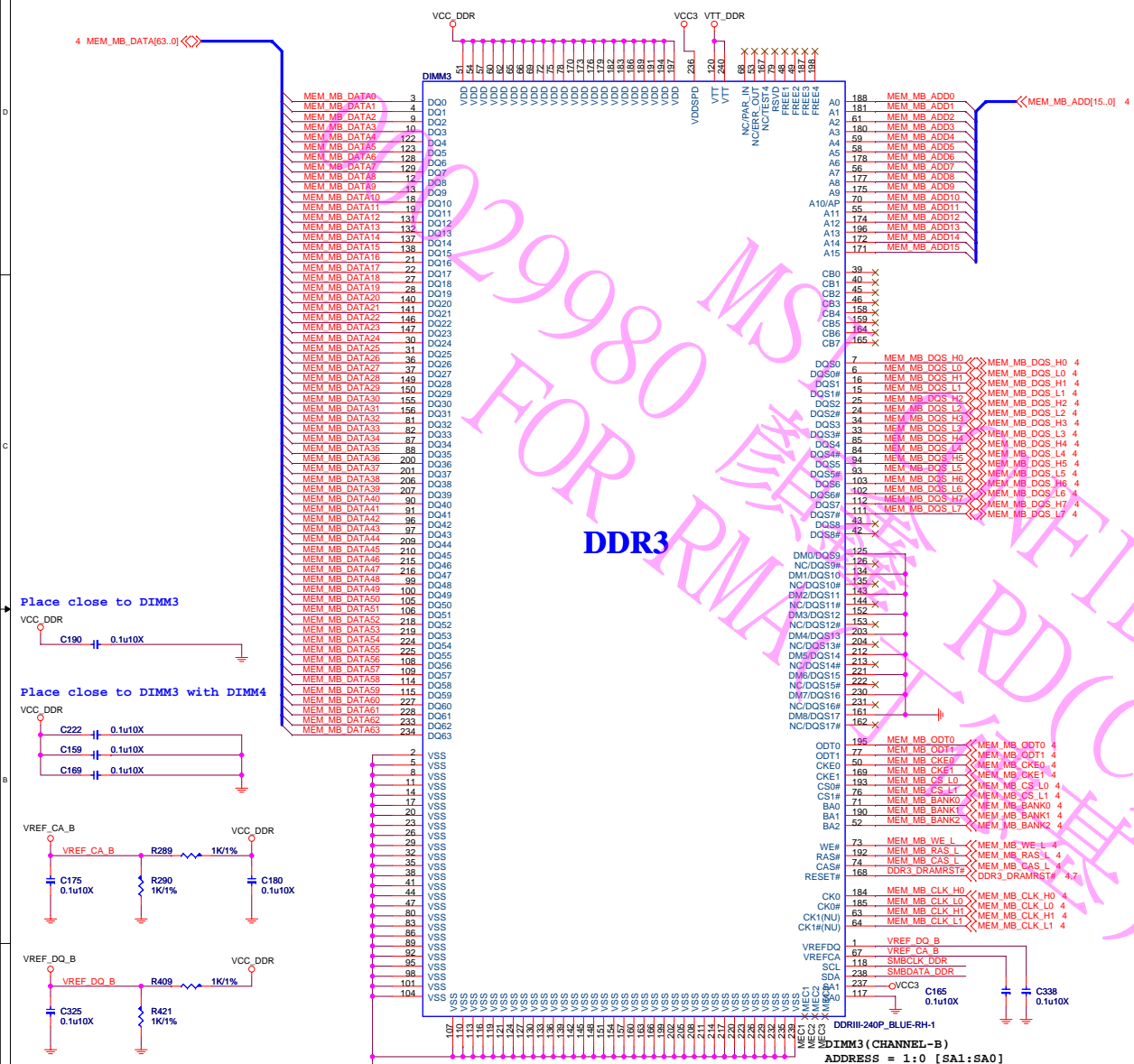


DDRIII DIMM_A0

DDRIII DIMM_A1

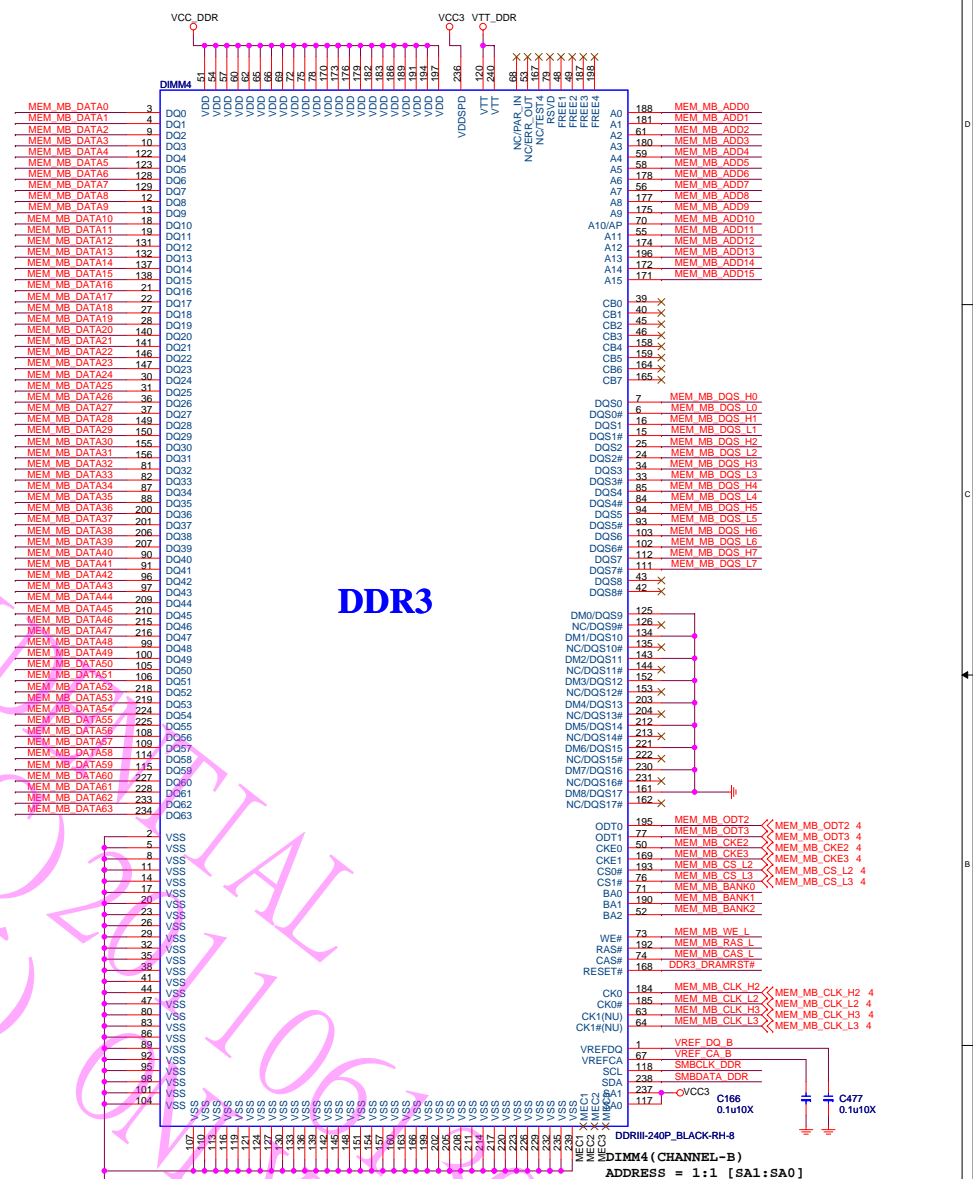


DDRIII DIMM_B0



DDR3

DDRIII DIMM_B1



DDR3

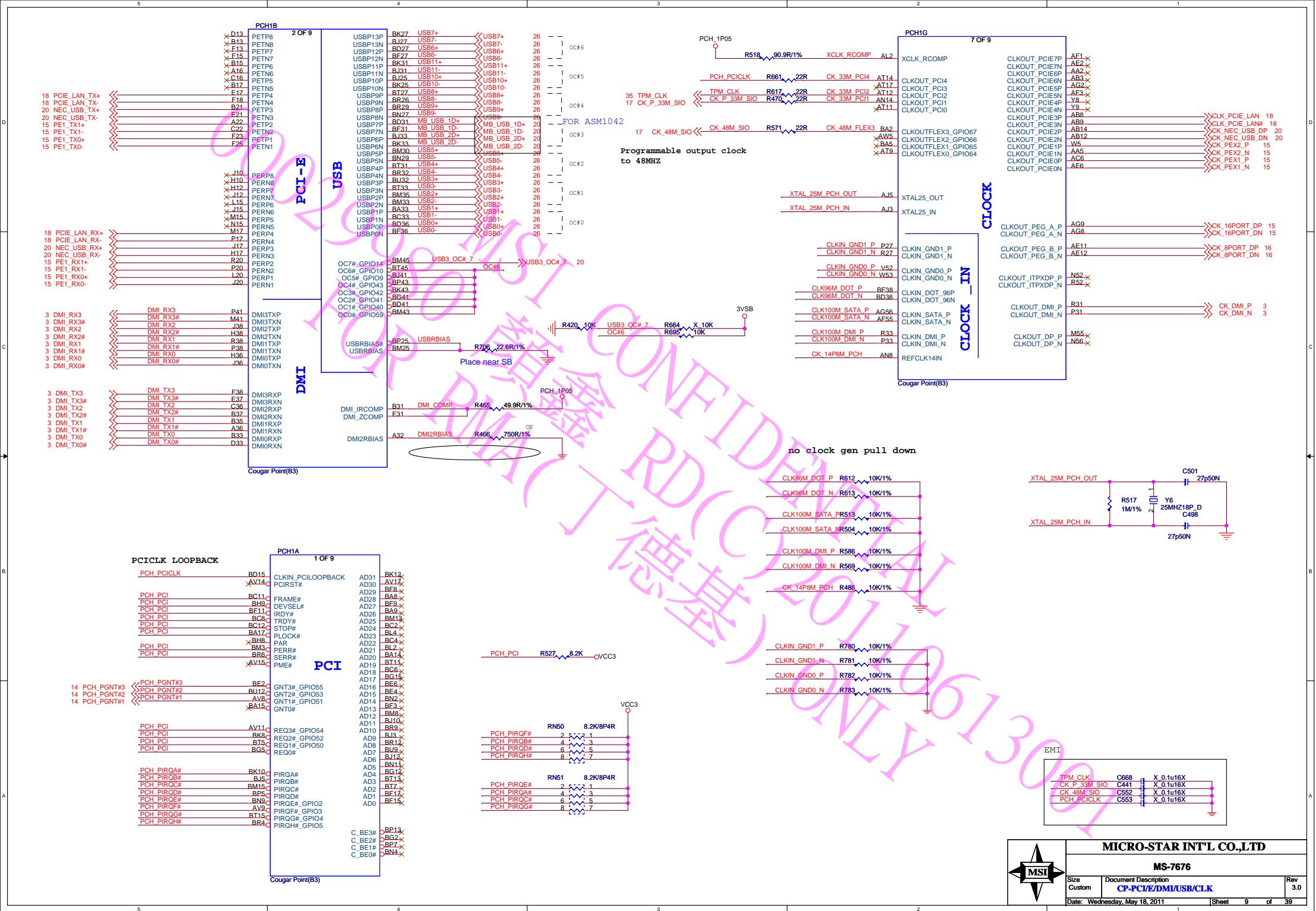
SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7



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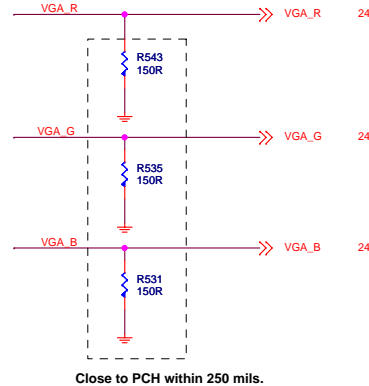
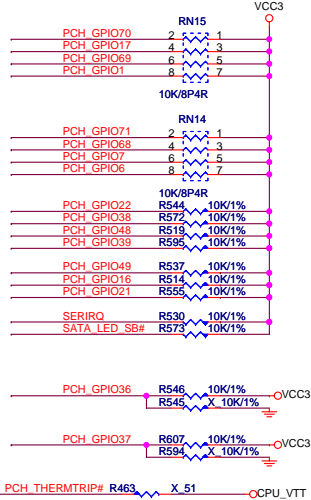
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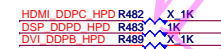




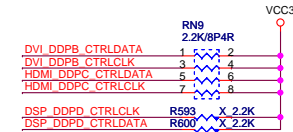
Pull HIGH for PCH



No VGA(pull down)



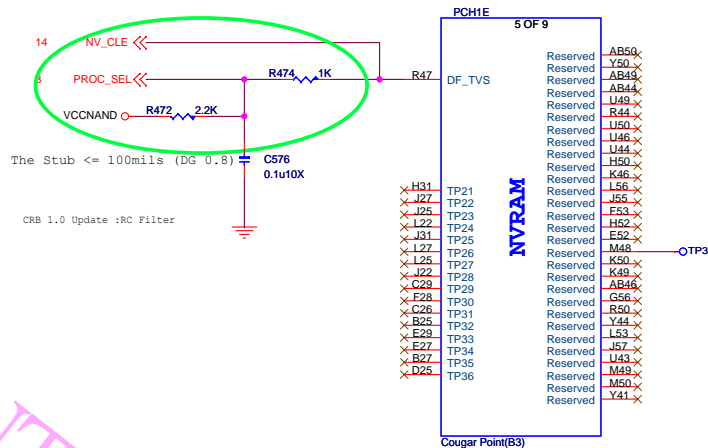
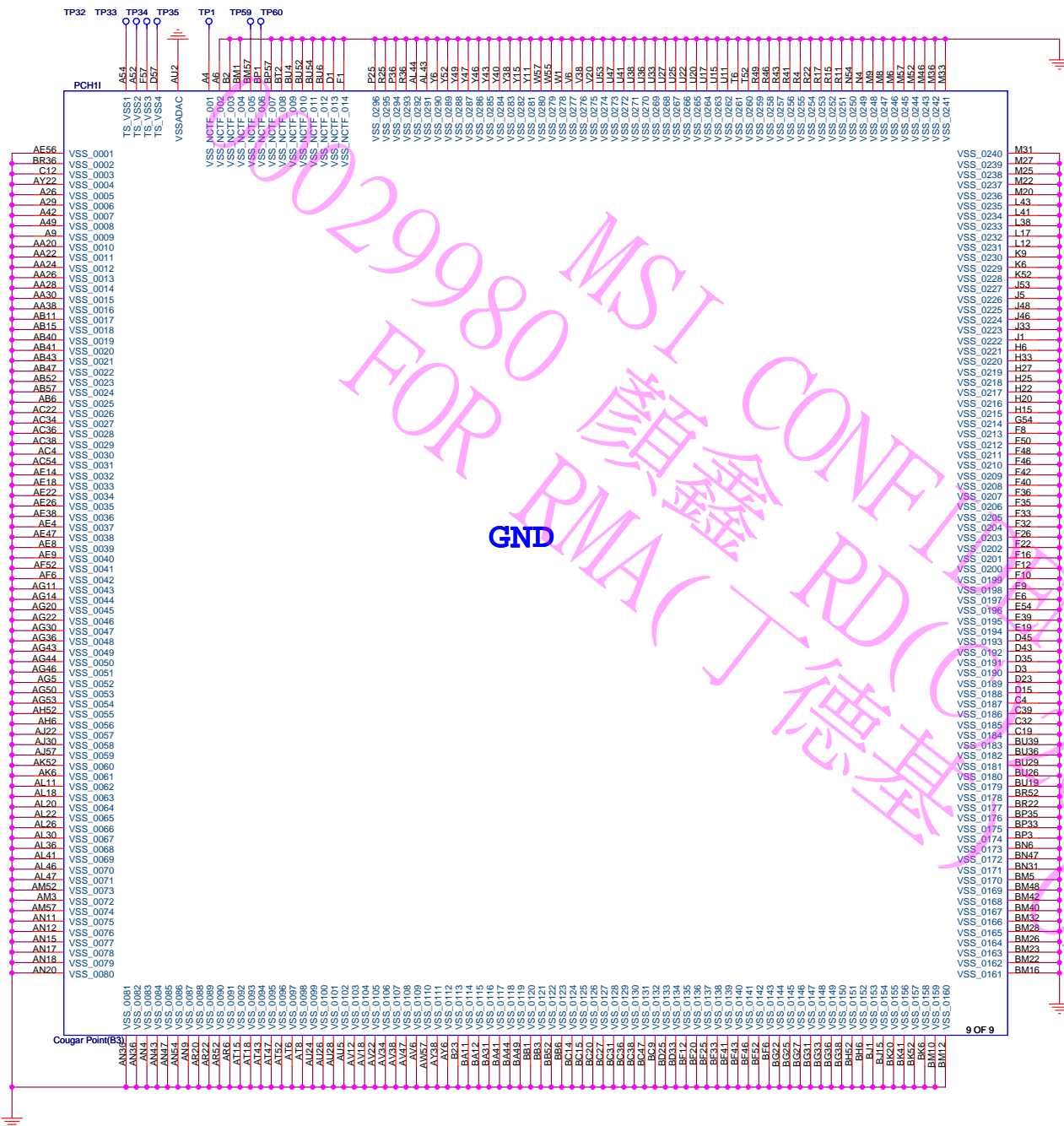
Enable VGA(CTRLCLK/DATA Pull High)



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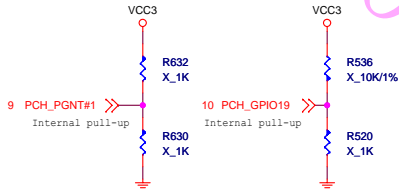
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



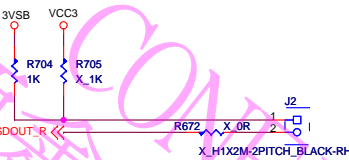
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



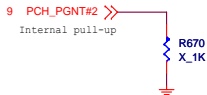
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.

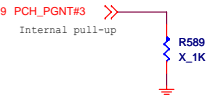


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

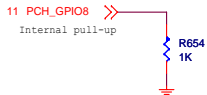
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



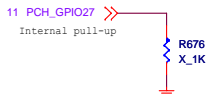
DMI AC/DC MODE
0 : AC
1 : DC *



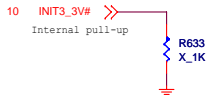
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

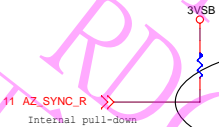


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

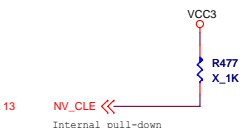
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



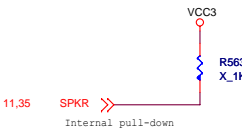
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS_CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS_CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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PCI_Express X16 slot

Trace width > 200 mils

PCI EXPRESS x1-PORT

PCI EXPRESS x1-PORT

SLOT-PCI164P_BLUE-2PITCH-RH-5

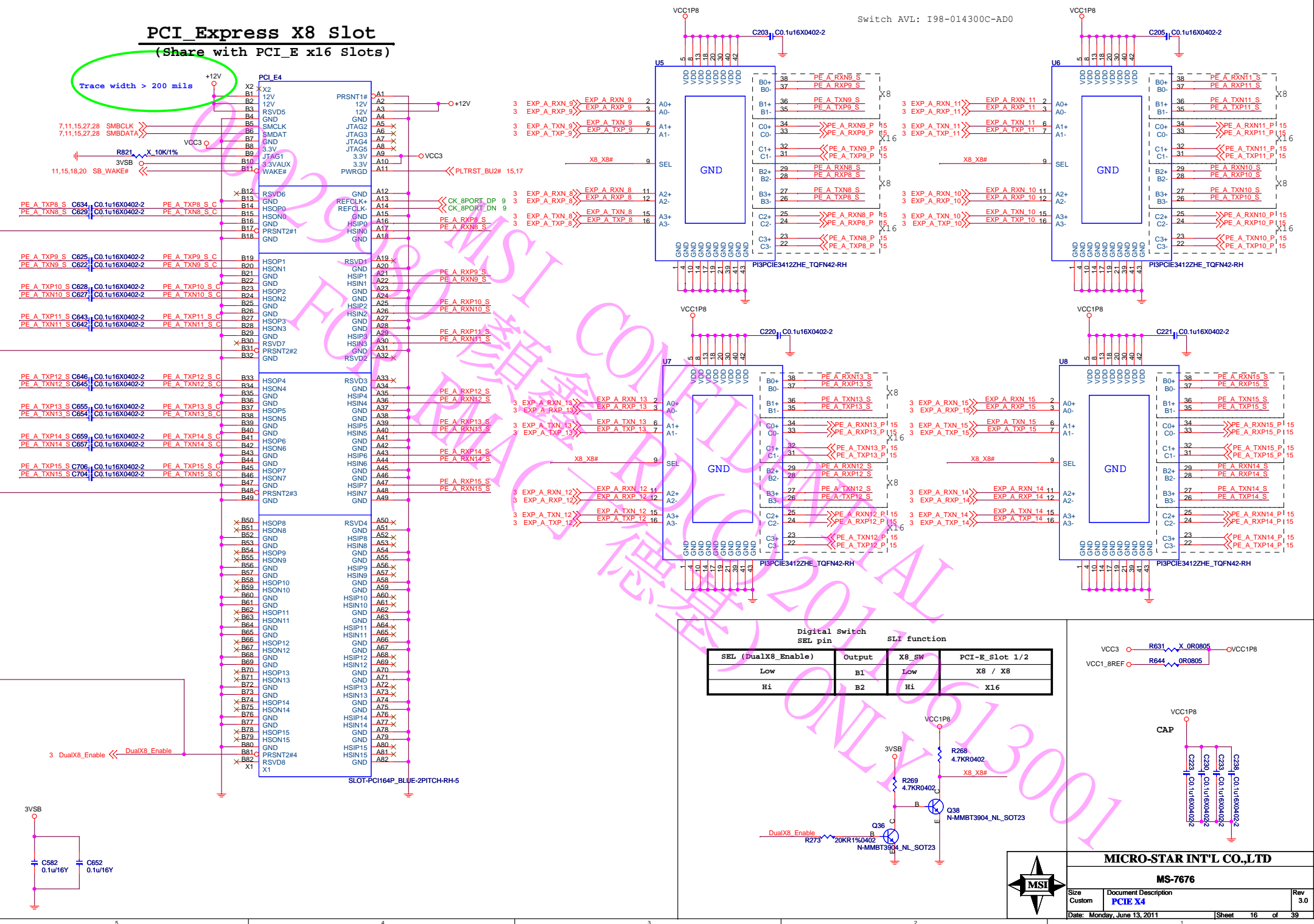
SLOT-PCI36P_BLACK-2PITCH-RH-10



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Custom	PCIe x16 x1/x1	3.0
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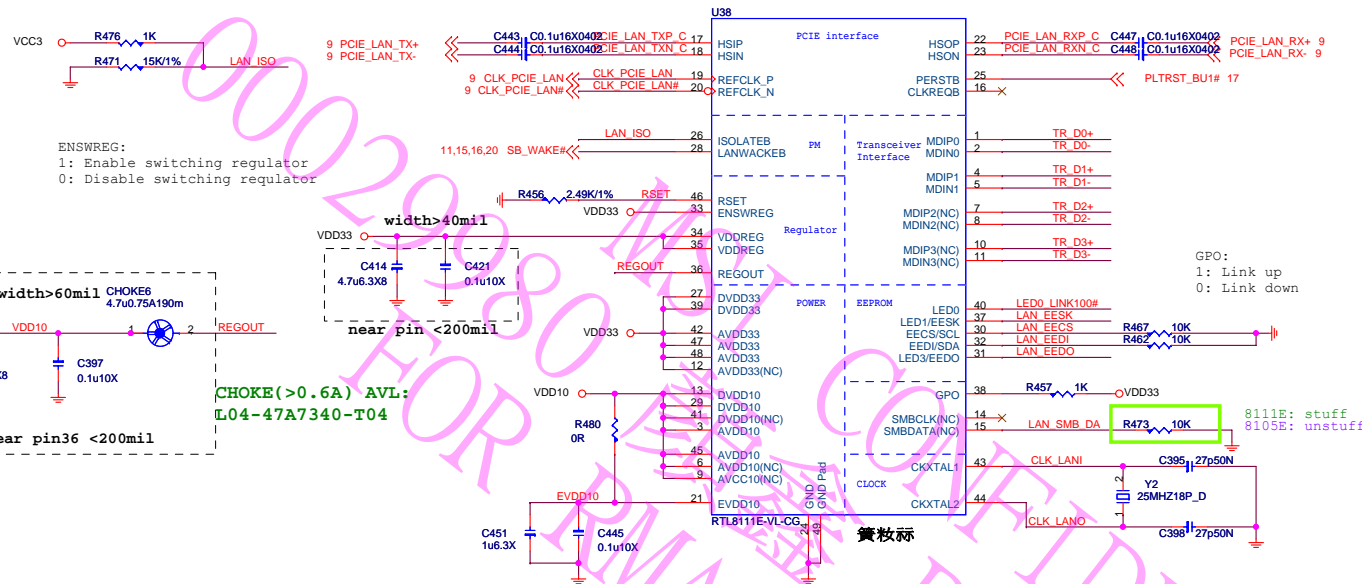
PCI Express X8 slot (Share with PCI_E x16 Slots)

Trace width > 200 mils



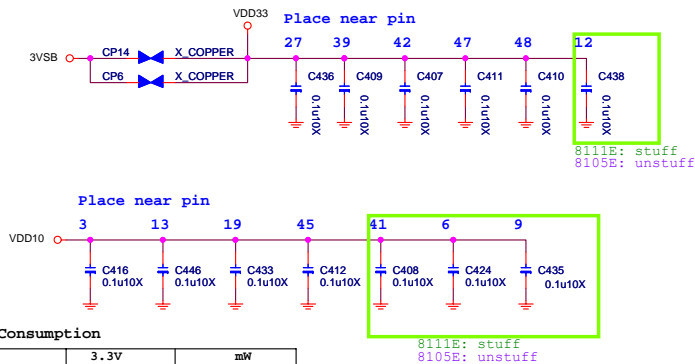
RTL8111E Giga LAN

RTL8105E 10/100M LAN



Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

3.3v Power on rise time : 1-100ms. MAX: 163mA

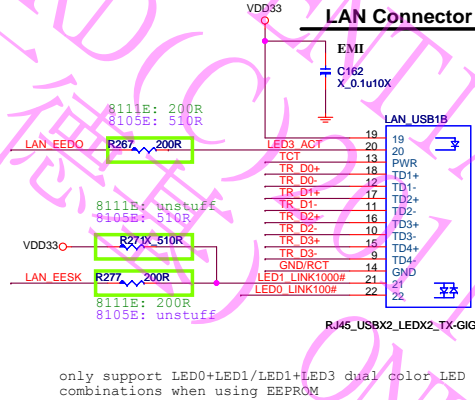


8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22

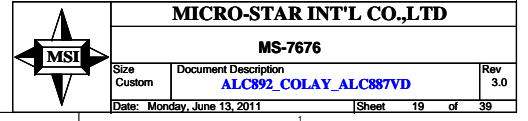
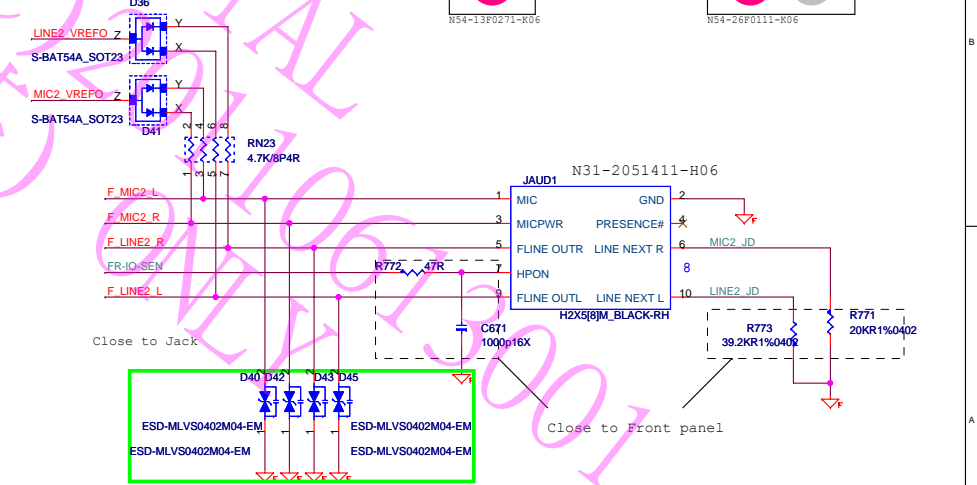
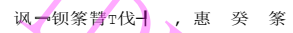
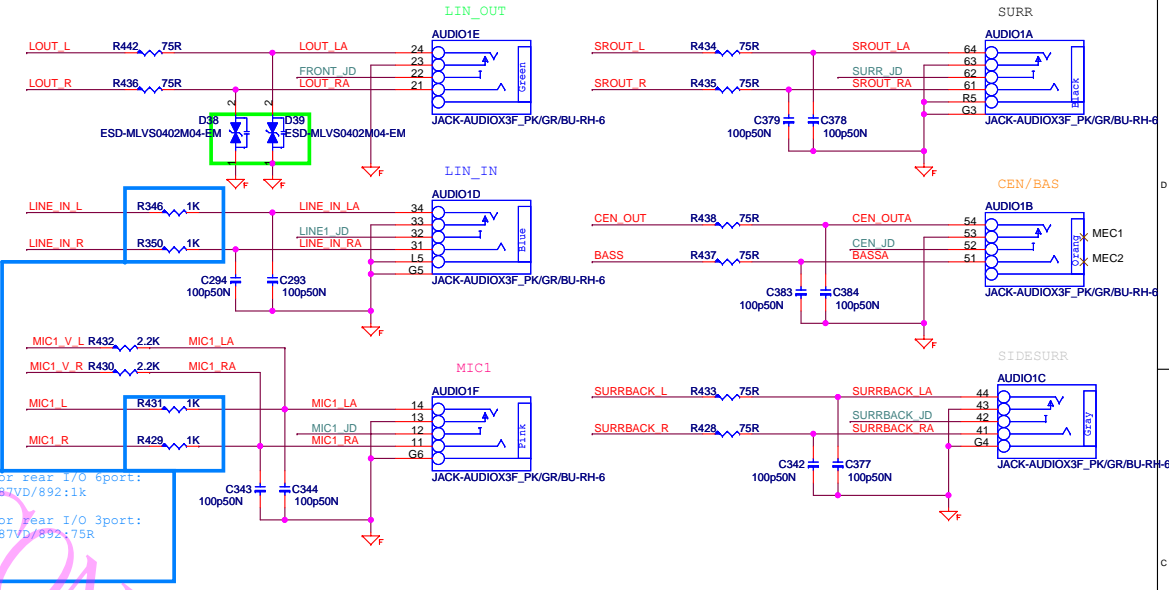
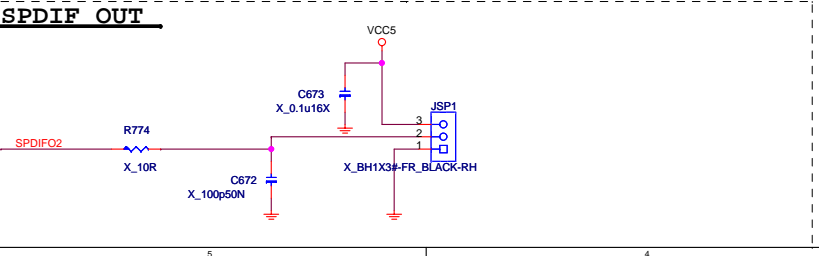
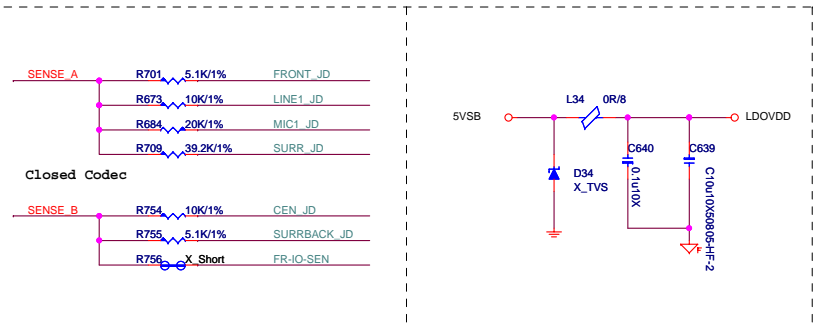
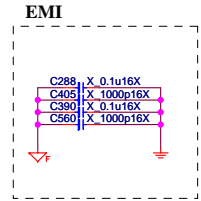
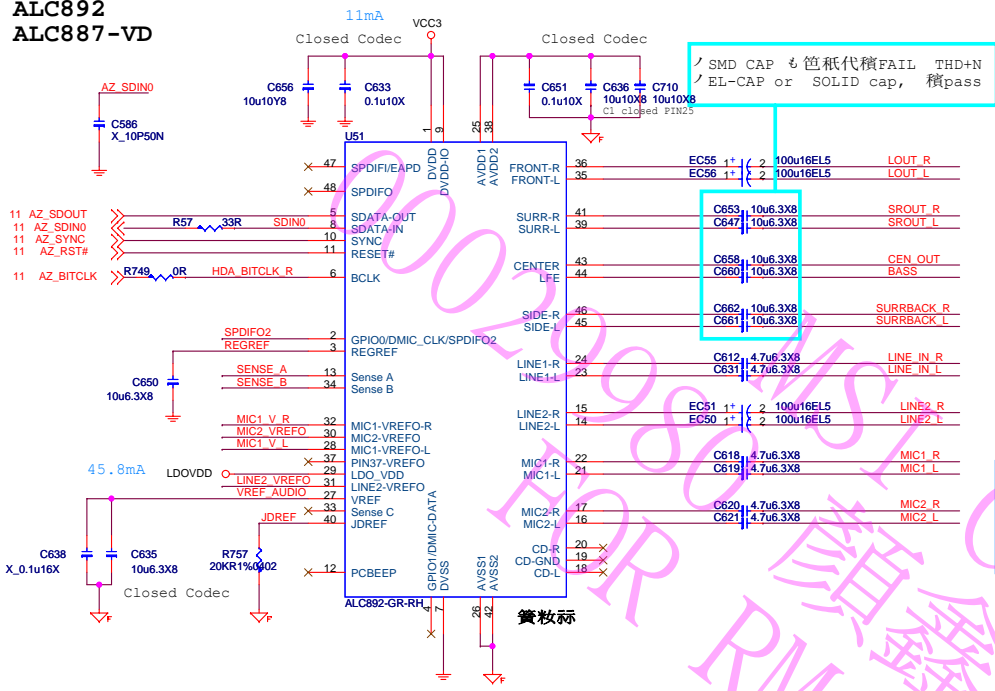


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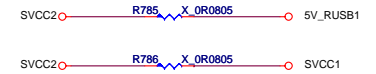
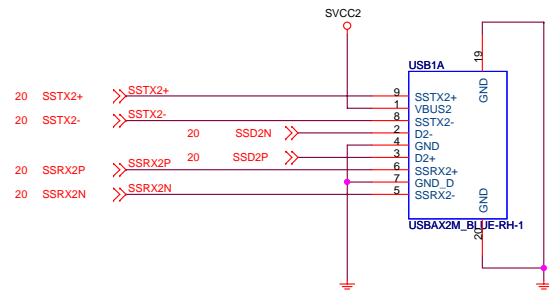
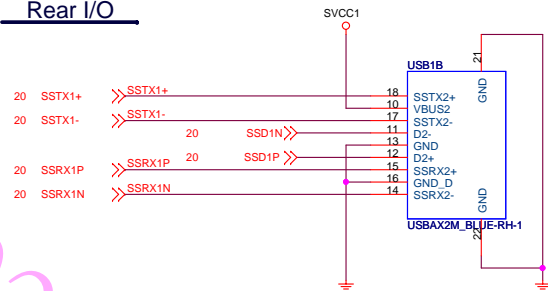
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ALC892
ALC887-VD

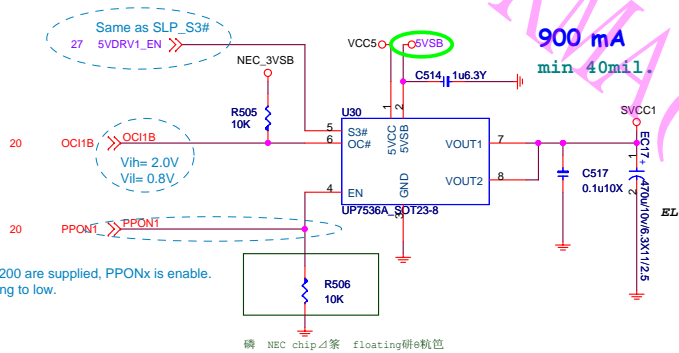
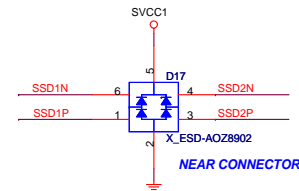


Rear I/O



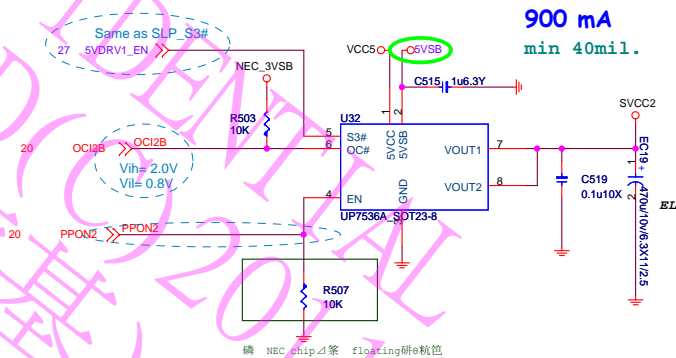
ESD Protection

Close to Connector



All power sources of uPD720200 are supplied, PPNx is enable.
PPONx is low when OC1x going to low.

請 NEC chip 案 floating 研 軌 芭



請 NEC chip 案 floating 研 軌 芭



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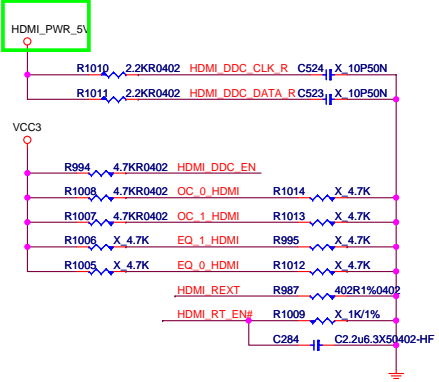
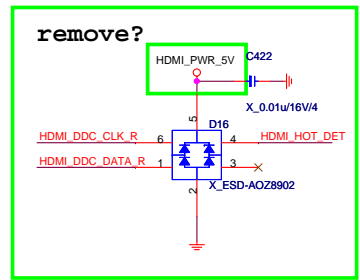
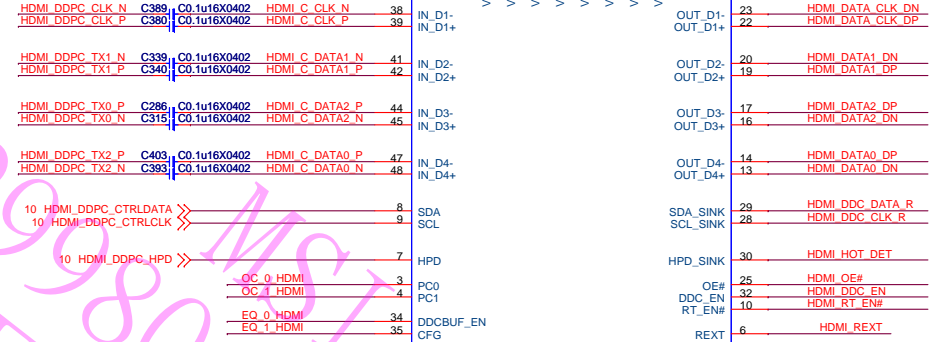
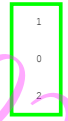
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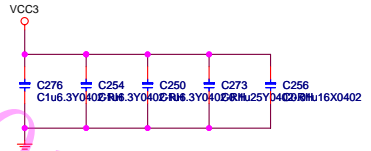
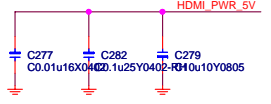
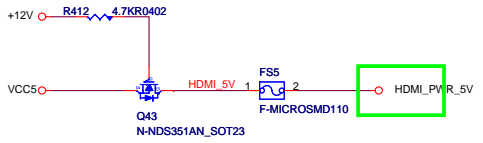
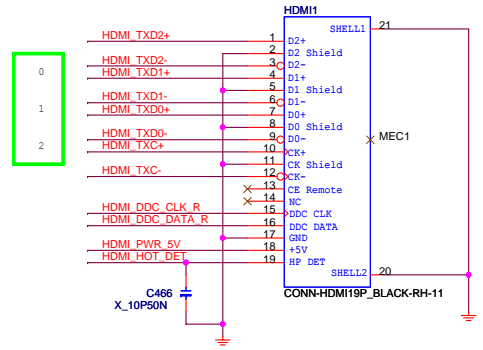
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



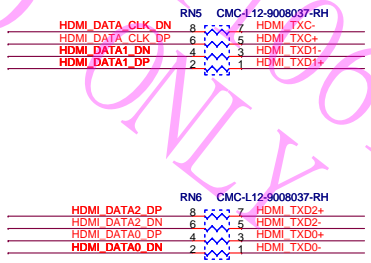
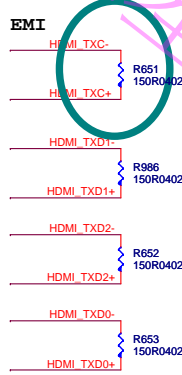
HDMI level shifter



PERICOM 腹:B0B-411LS2C-P22.
PARADE 腹:B0B-081010C-P97.



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.



[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

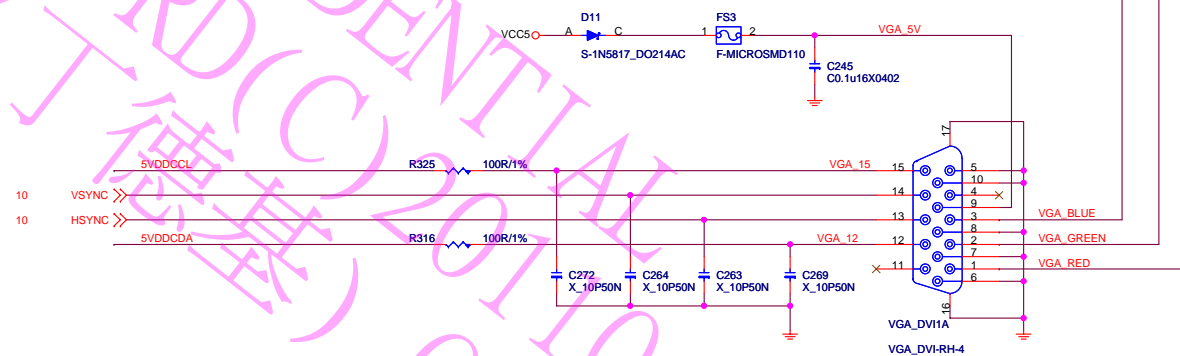
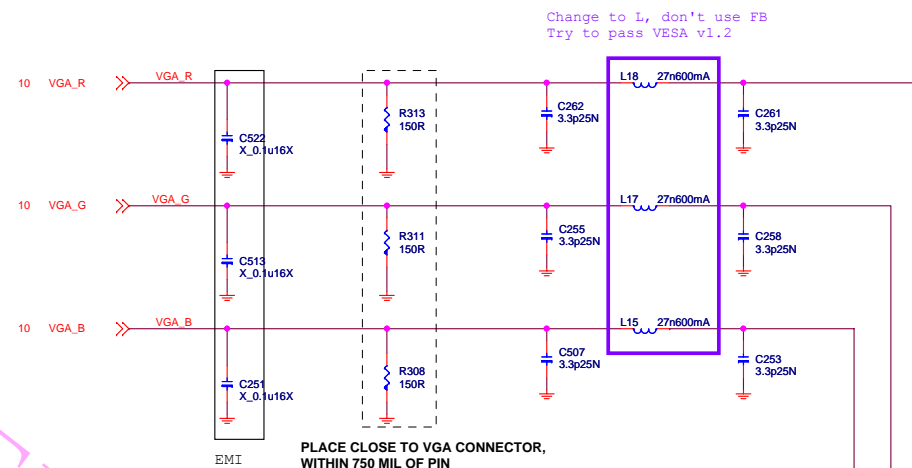
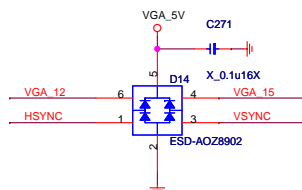
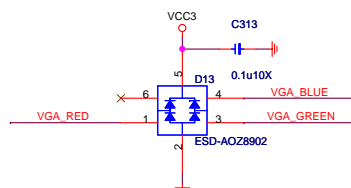
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

[illegible]

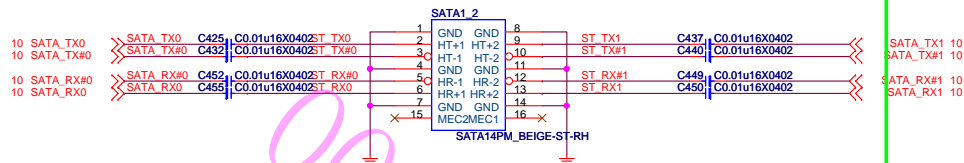
MICRO-STAR INT'L CO.,LTD

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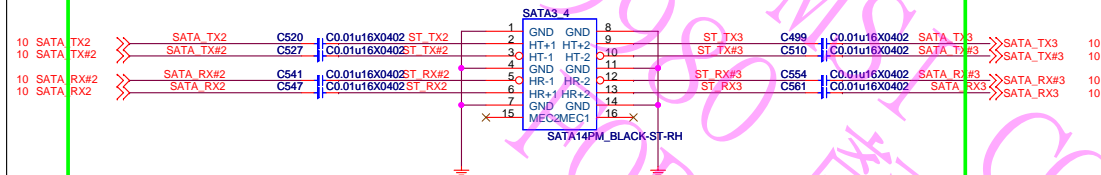
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SATA 6G PORT 0,1

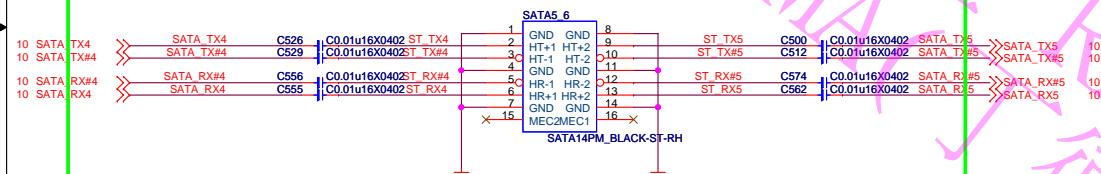
H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G



SATA 3G PORT 2,3

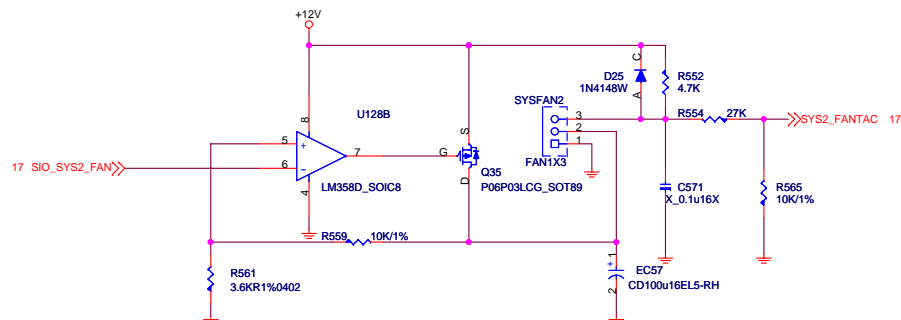


SATA 3G PORT 4,5

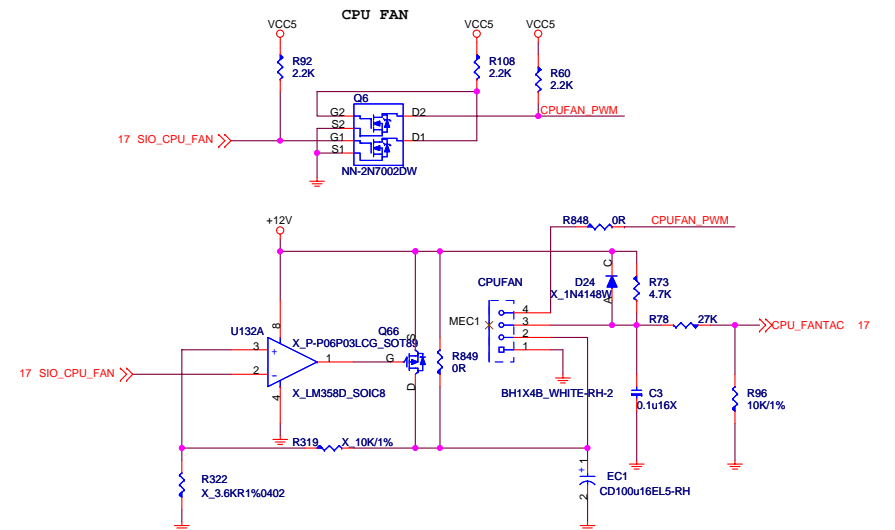


SYSTEM FAN-CONTROL CIRCUIT

SYSTEM FAN2

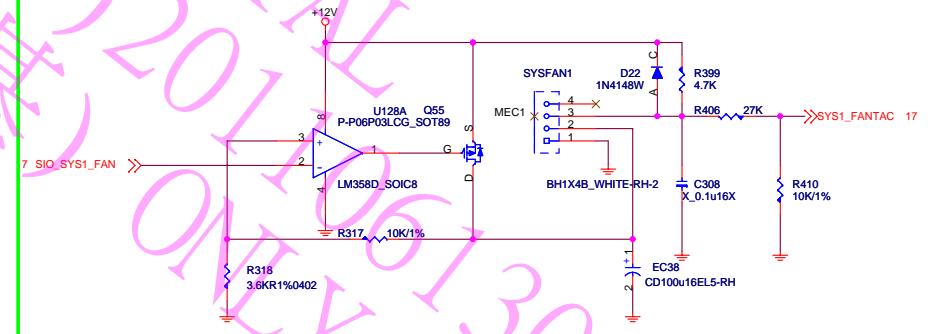


CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT

SYSTEM FAN1

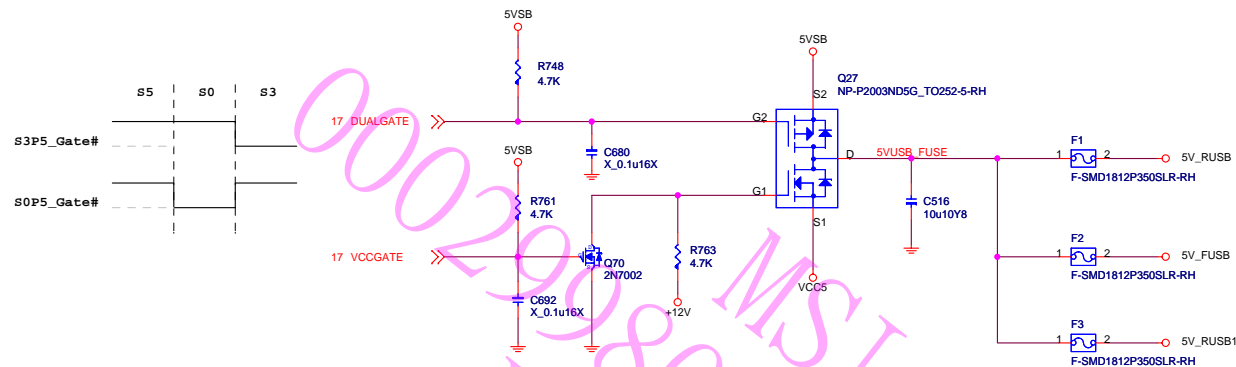


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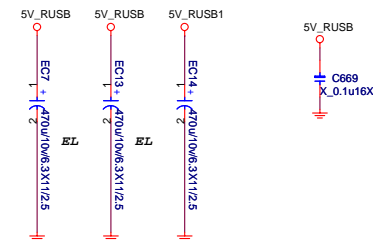
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5V_RUSB Switch

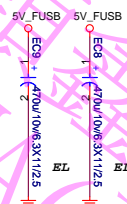


NEAR USB REAR CONNECTOR



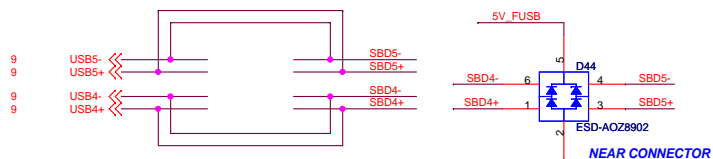
Front USB Connector

NEAR USB Front CONNECTOR

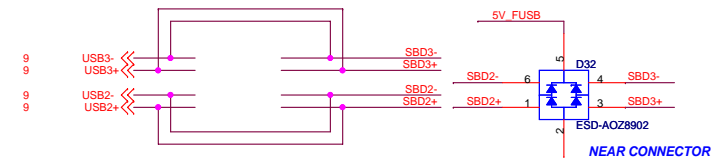


For H61 6,7,12,13 Port should be remove

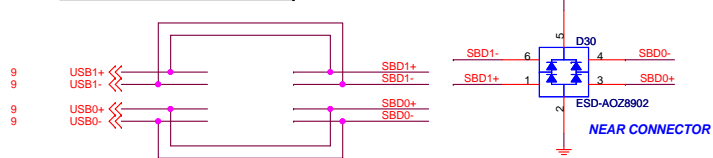
FRONT USB PORT 4,5



FRONT USB PORT 2,3

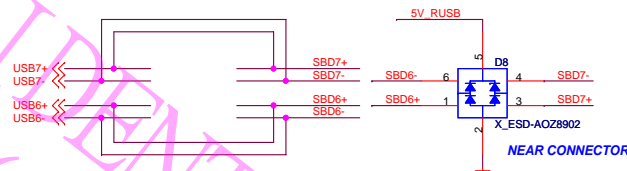


FRONT USB PORT 0,1

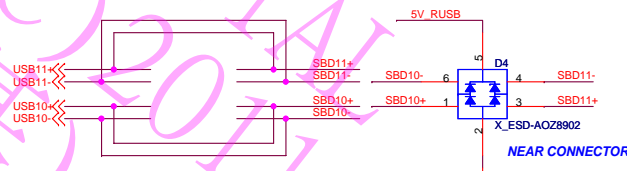


Rear USB Connector

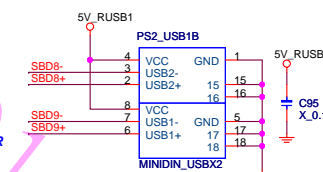
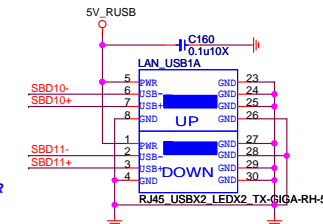
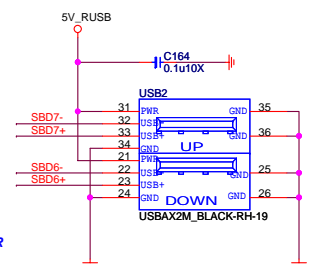
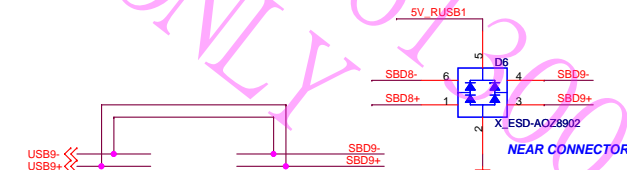
REAR USB PORT 6,7 (With HDMI)



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)

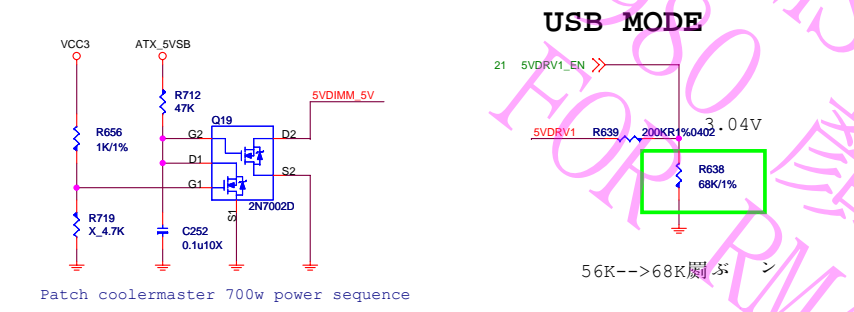
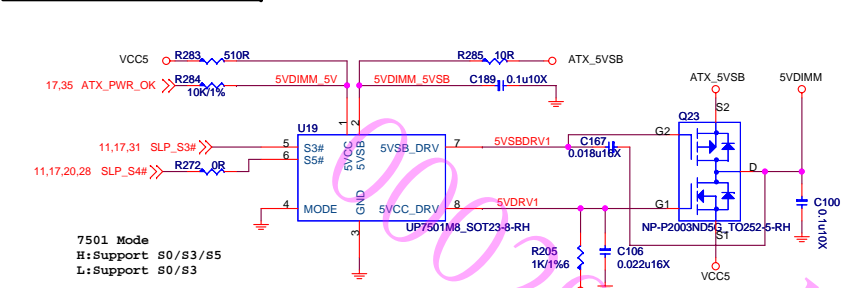


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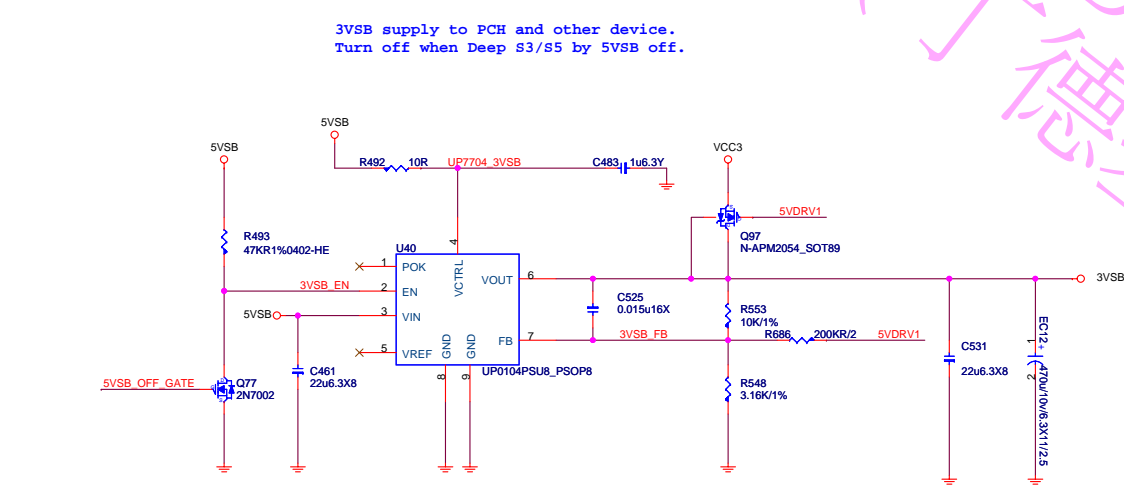
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Size	Document Description	Rev
Custom	USB Connector	3.0
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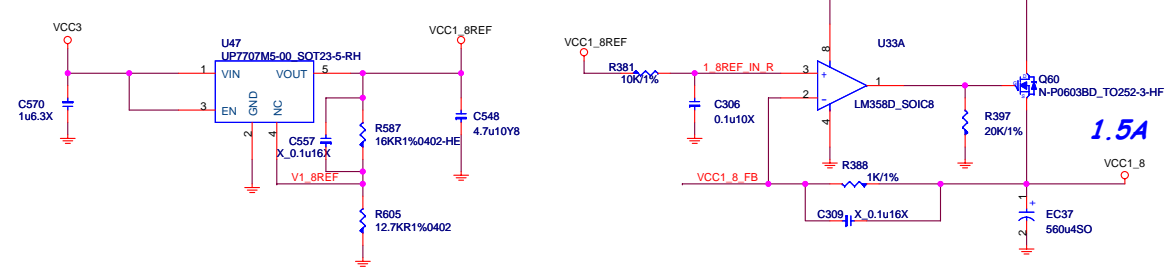
5VDIMM FOR DDR



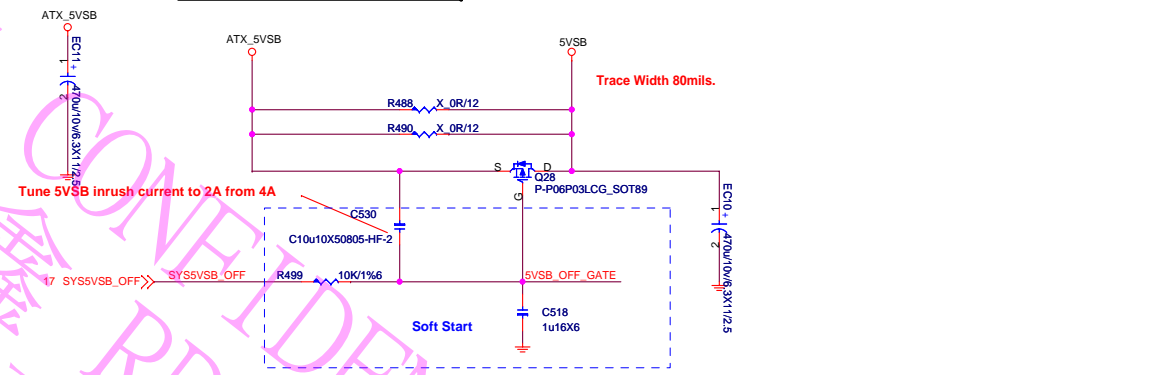
3VSB



VCC1_8REF



5VSB Power Switch



UPI VOLTAGE CONSOLE

0x2A: RL=10K, RH=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

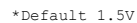
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Size: Custom | Document Description: ACPI controller UPI | Rev: 3.0

Date: Thursday, June 02, 2011 | Sheet: 27 of 39

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT

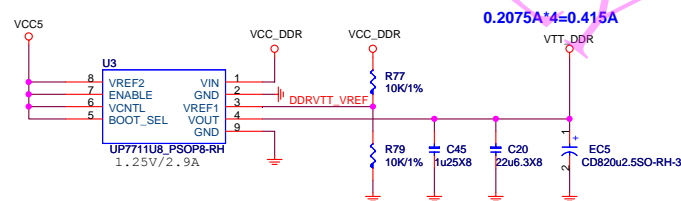


DDR OV1	=	GPI001 (S/IO)
DDR-OV2	=	GPI002 (S/IO)



0x20: RH=10K, RL=OPEN

P.S. Only for meet Intel power down sequence.


$$0.2075A \times 4 = 0.415A$$


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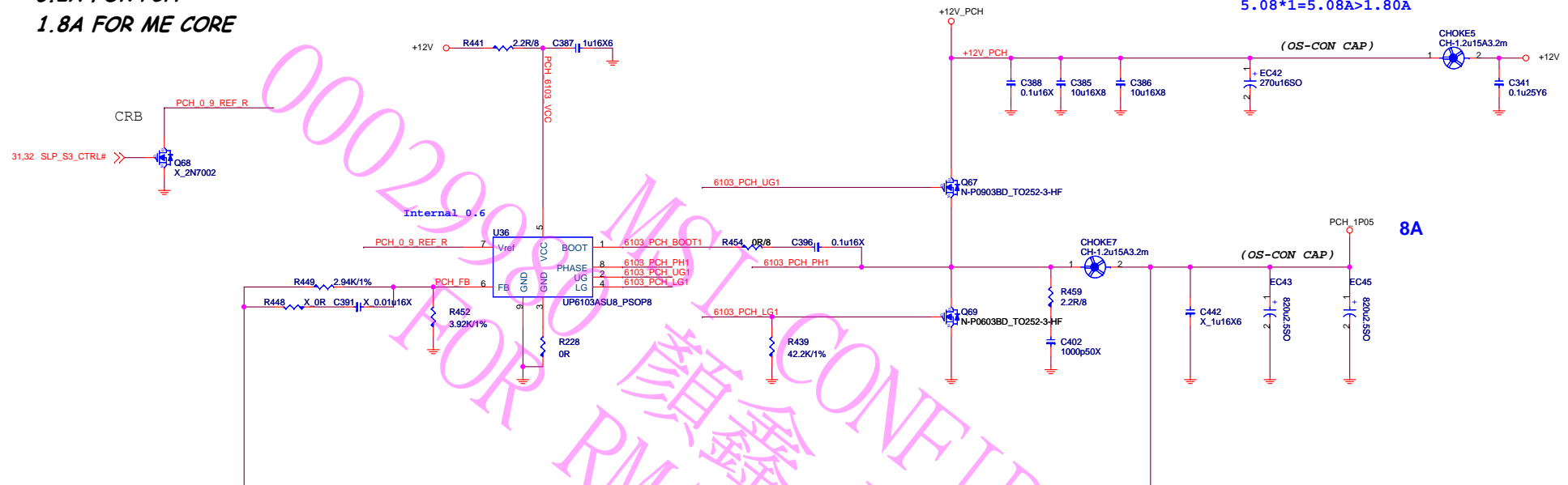
Size Custom	Document Description DDR Power - uP6103 1-Phase	Rev 3.0
Date: Thursday, June 02, 2011		Sheet 28 of 39

PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE



Iripple=1.80A
5.08*1=5.08A>1.80A

8A



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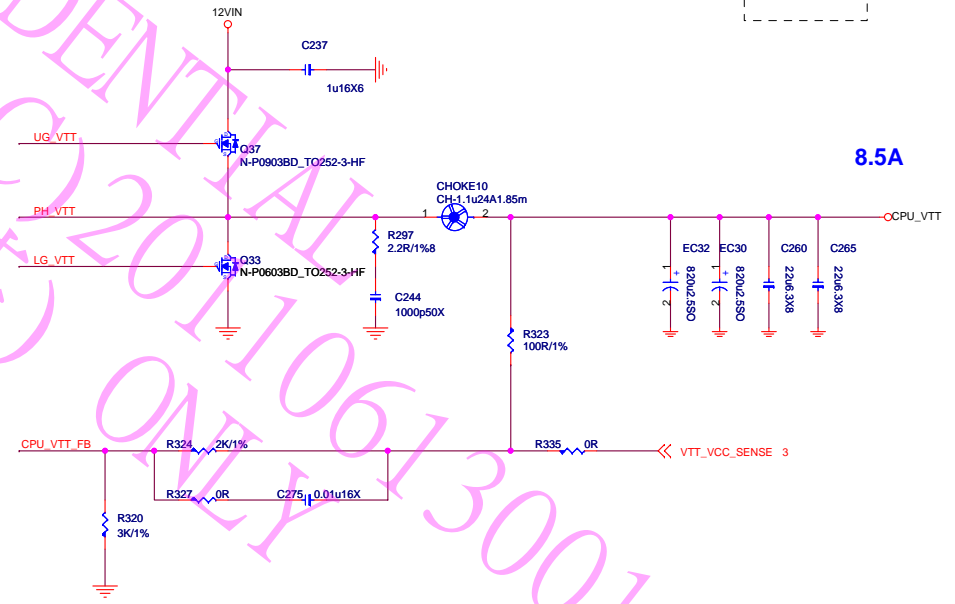
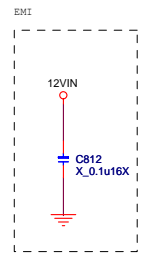
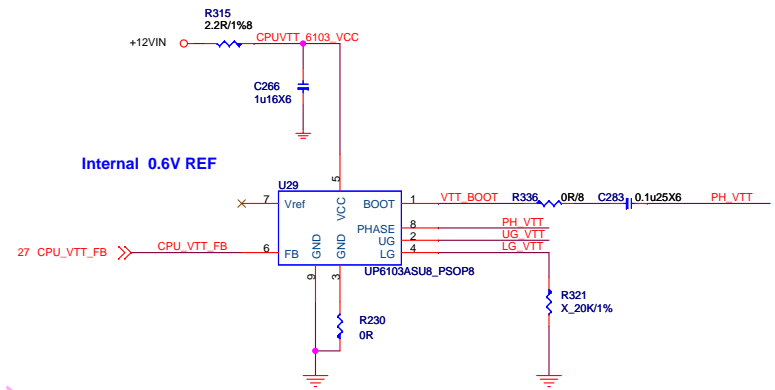
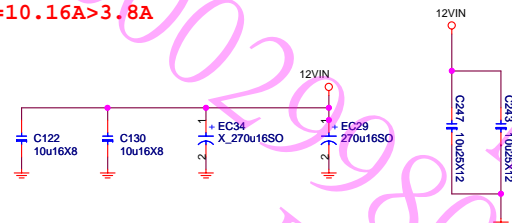
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Size	Document Description	Rev
Custom	PCH Power - uP6103 1-Phase	3.0
Date:	Sunday, May 29, 2011	Sheet 29 of 39

CPU_VTT:1.05/1.00

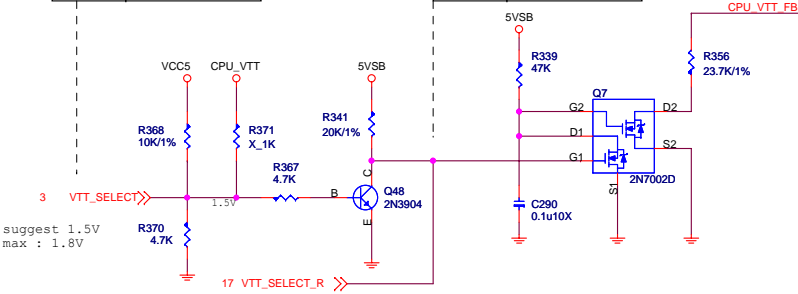
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$


$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V





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Size: Custom

Document Description: CPU_VTT - uP6103- 1-Phase

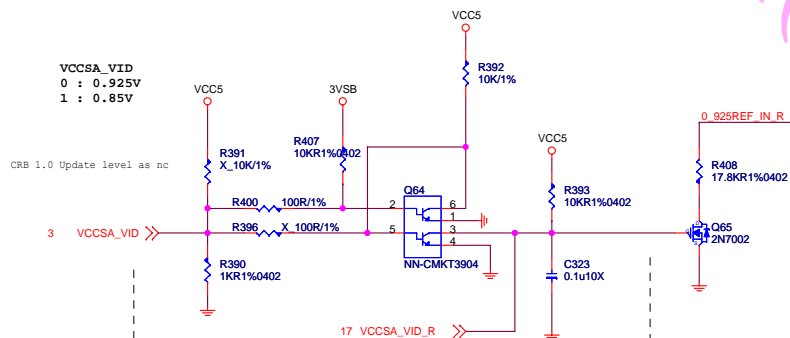
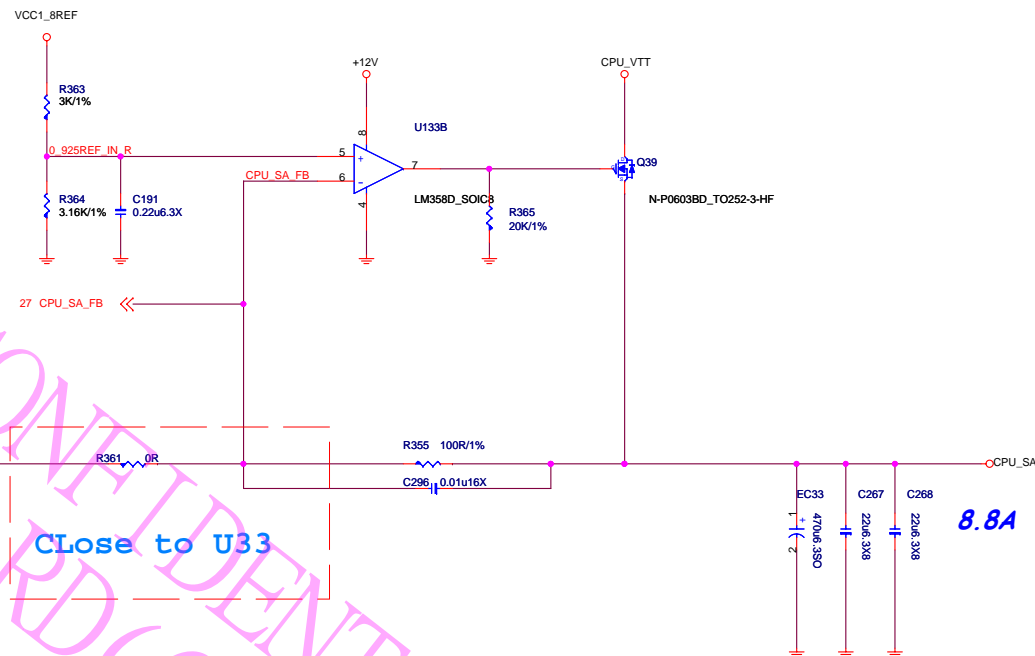
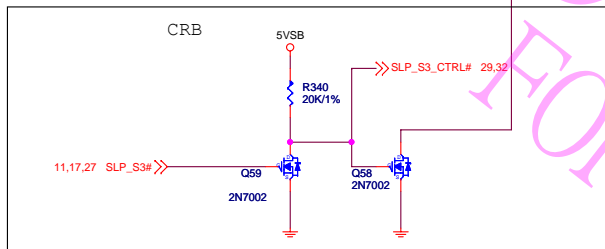
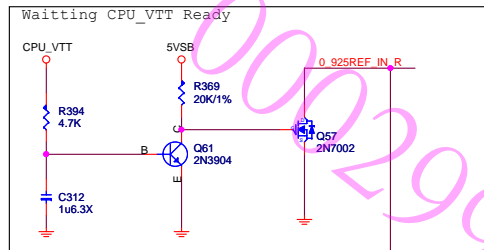
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CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

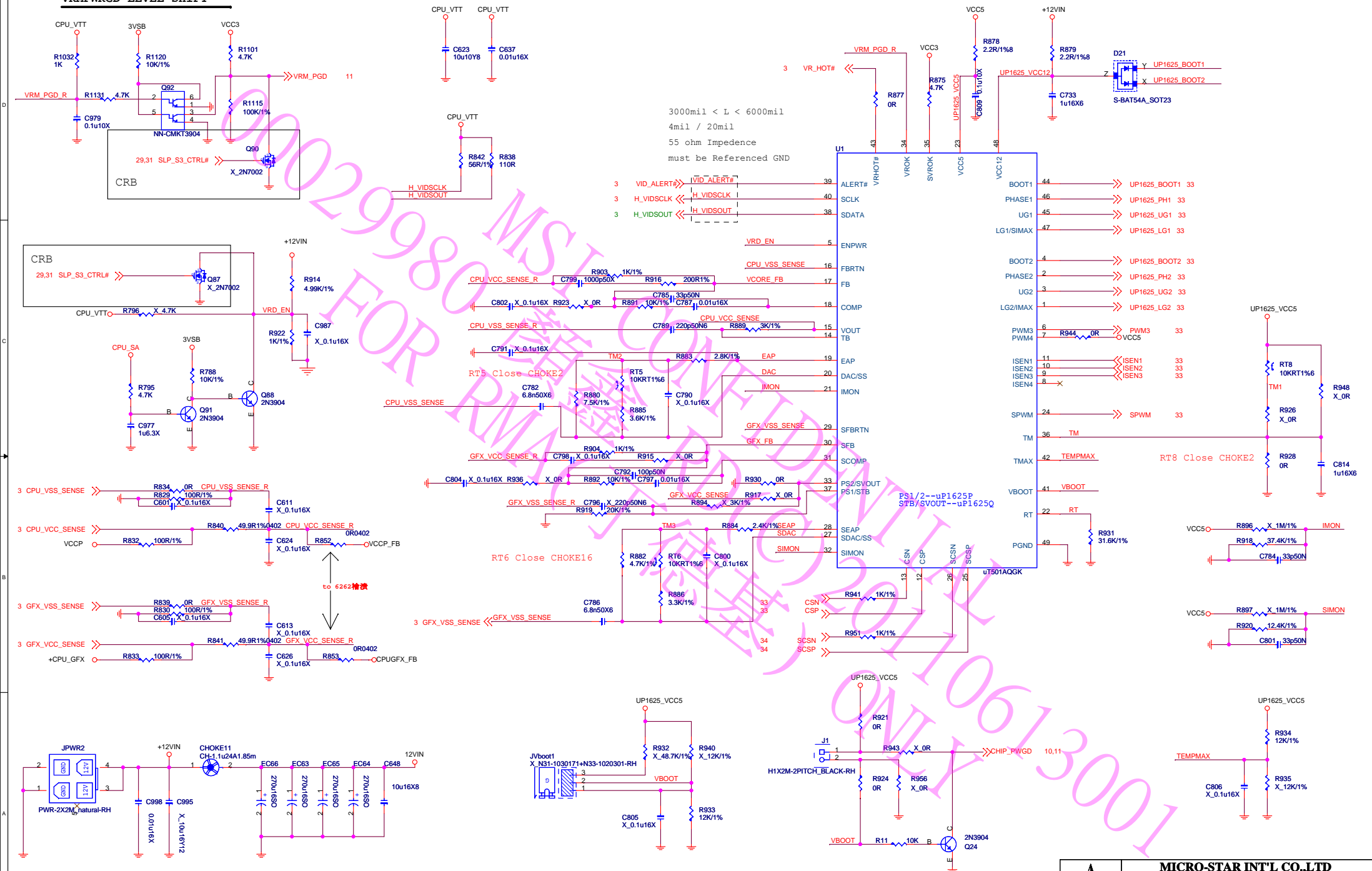


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Size	Document Description	Rev
Custom	CPU_SA - uP6103 1-Phase	3.0
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VRMPWRGD LEVEL SHIFT



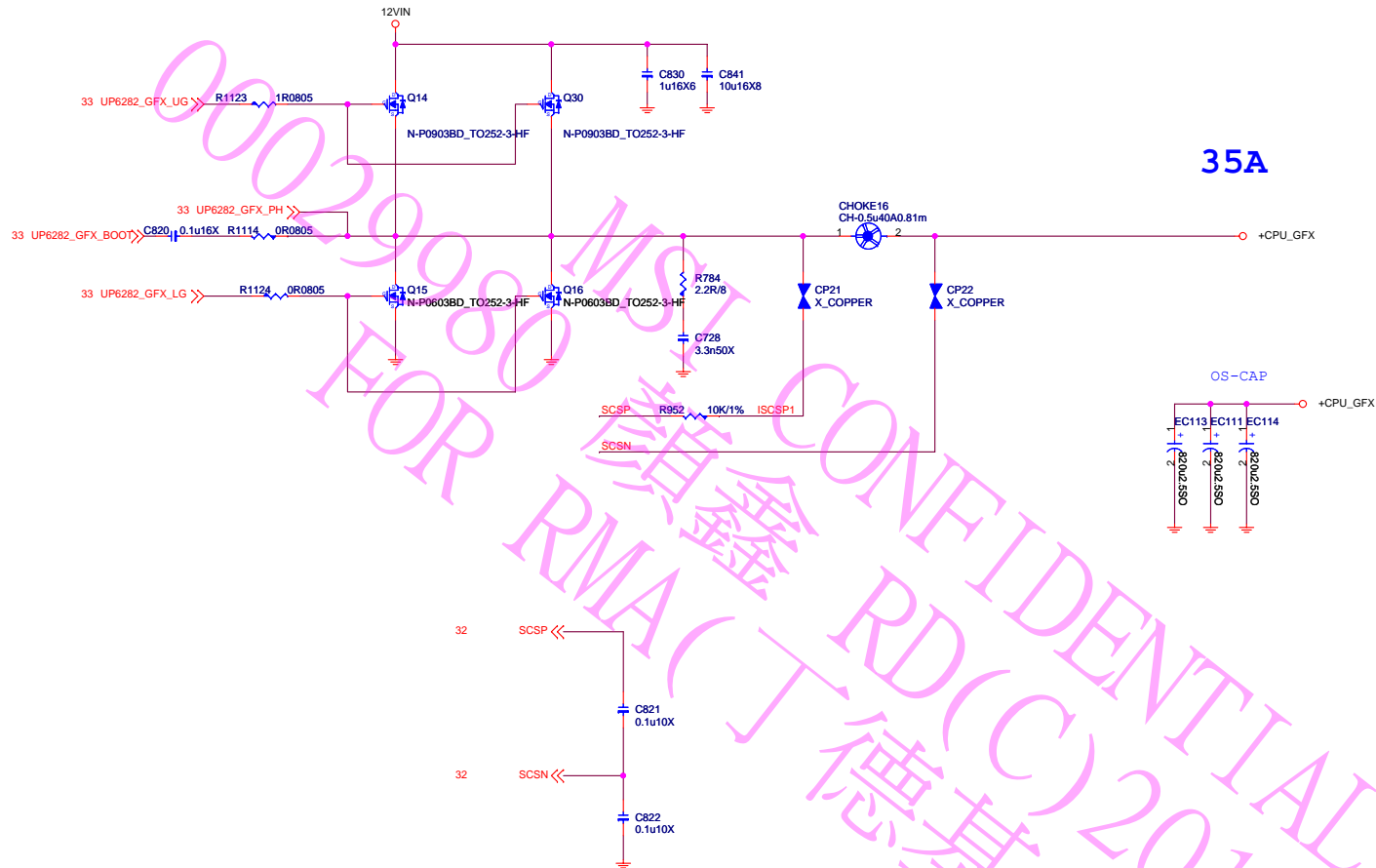
```
Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24
```



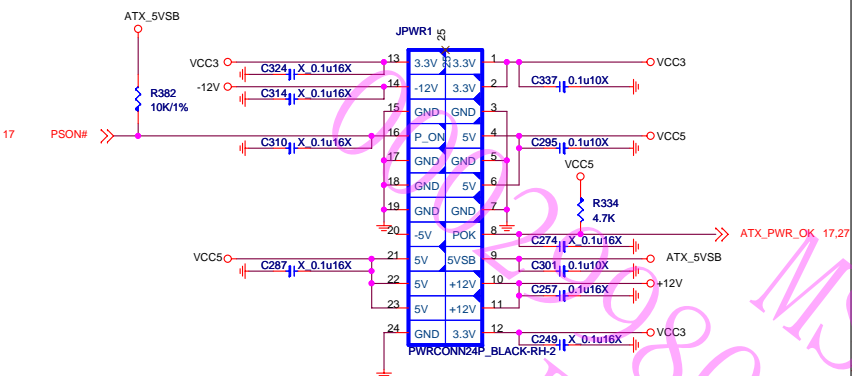
MICRO-STAR INT'L CO.,LTD

MS-7676

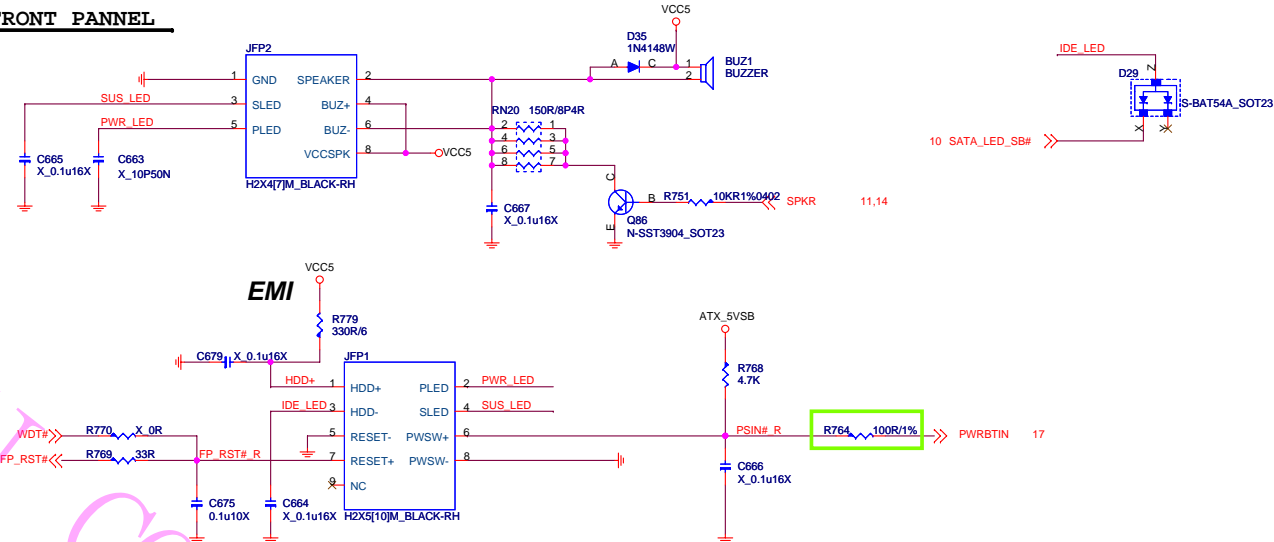
Size Custom	Document Description VRD12 - UPI6234 6+1-Phase	Rev 3.0
Date: Sunday, May 29, 2011		Sheet 32 of 39



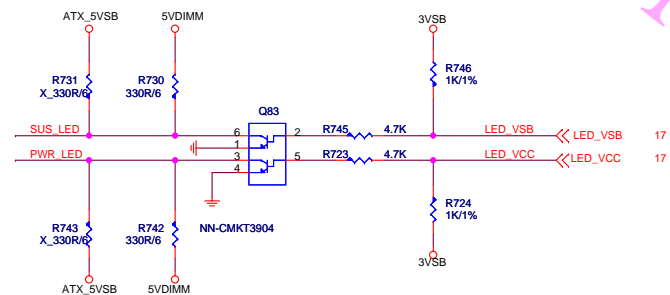
ATX POWER CONNECTOR



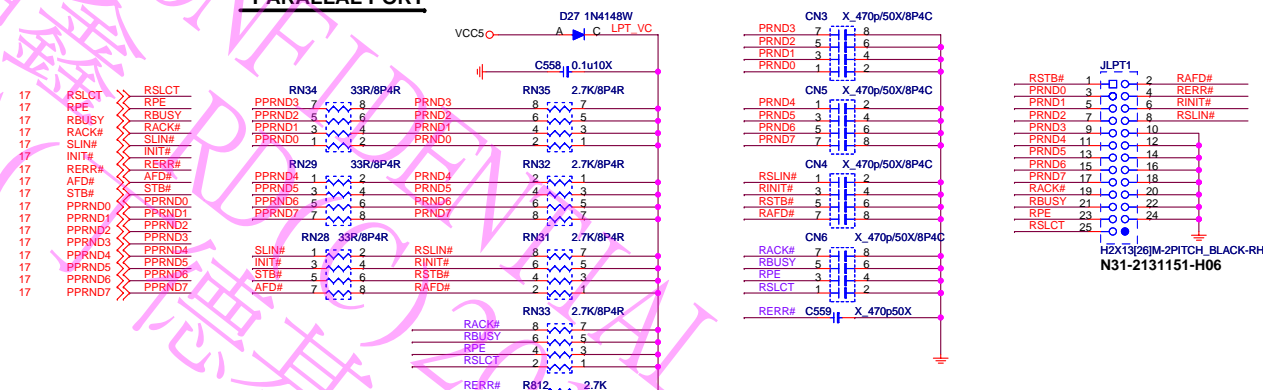
FRONT PANNEL



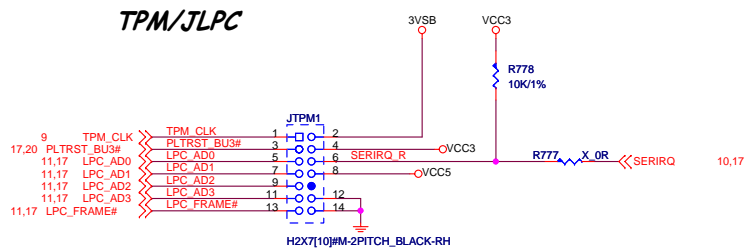
LED (for Fintek 71869)



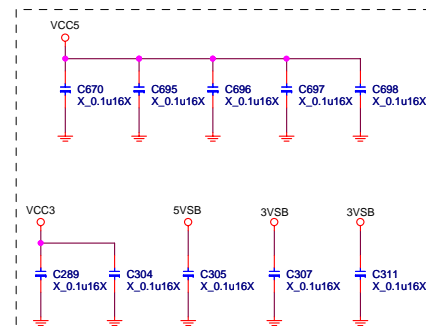
PARALLAL PORT



TPM/JLPC



EMI



MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description ATX PWR-Connector & Front Panel & EMI	Rev 3.0
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MS-7680-4.0

OPT	Configure	BOM	Function
	H61MU-S01 (B3)	601-7680-120	MS-7680 40 H61MU-S01 (B3), H61+2DDR3+1*PCI_Ex16+3*PCI_Ex1+4*SATAII+HD 8CH Audio+10USB2.0+2USB3.0+Gb LAN, (EuP), RoHS
A	H61MU-E34 (B3)	601-7680-11S	MS-7680 40 OPT:A H61M-E34 (B3) Intel H61+2*DDRIII+1*PCIe16, 2*PCIe1, 1*PCI+ DVI/D-sub/HDMI+4*SATAII+10*USB2+HD8Ch Audio+Gb lan, EuP, (All Solid Cap), RoHS

00029980 MSI

FOR RMA

MSI

CONFIDENTIAL

2013/07/30

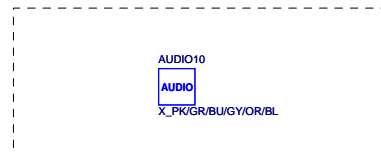
ONLY

MSI

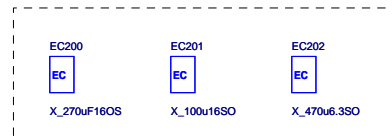
CONFIDENTIAL

2013/07/30

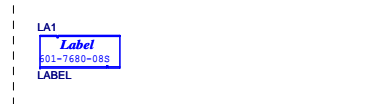
AUDIO CON OPT.



EL/OS OPT.



LABEL OPT.



PK0-0768040-E36, E3E, 23, 脚
吹邻缸 (MSIS), 4, Coffee
PK0-0768040-E36, E3E, 27, 脚
吹邻缸 (MSIS), 4, Coffee
PK0-0768040-G37, 弘e, 23, 脚
吹邻缸 (MSIS), 4, Coffee
PK0-0768040-G37, 弘e, 27, 脚
吹邻缸 (MSIS), 4, Coffee



BAT-BCR2032P-RH



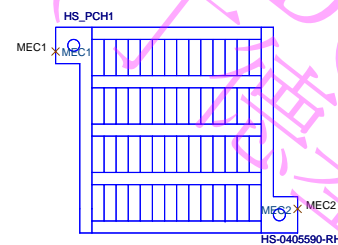
Rubber



Rubber

CPU
E21-7557050-L06

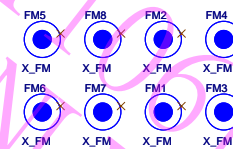
PCH XDP PWRGD/RESET



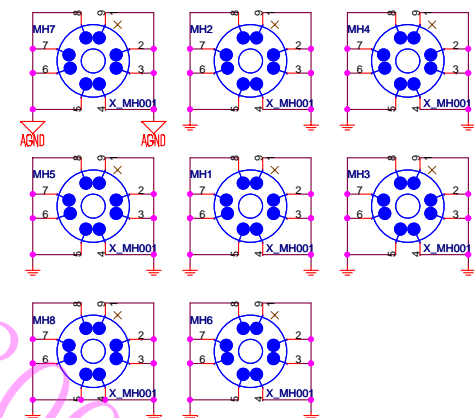
Simulation



Optical Fiducial Marks-120



Mounting Holes



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Custom	XDP / Manual Parts	3.0
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